(12) UK Patent Application (19) GB (11) 2 249 889 (13) A

(43) Date of printing by UK Office 20.05.1992

(21) Application No 9120516.1

(22) Date of filing 25.01.1991

(30) Priority data
(31) 02016473 (32) 26.01.1990 (33) JP

(86) International application data
PCT/JP91/00085 Jp 25.01.1991

(87) International publication data
WO91/11811 Jp 08.08.1991

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(51) INT CL[6] (as given by ISA)
G11C 27/00, A63F 9/22, G10K 15/04, G11C 5/00

(52) UK CL (Edition K)
H3H HGW
U1S S1172 S1945

(56) Documents cited by ISA
JP 63253755 A JP 63040898 U JP 61058679 A
JP 56116138 A JP 10185900 A

(58) Field of search by ISA
INT CL[5] A63F 9/22, G06F 3/16 13/38 15/44, G10K 15/04 G11C 5/00 27/00
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(54) Digital sound source device and external memory cartridge used therefor

(57) A digital sound source device which includes a semiconductor memory coupled to a central processing unit, the memory having a quantized data storage area and a program data storage area. A series of quantized data sequences and stop codes are stored in a series of locations in the quantized data storage area, and a start address is set in a particular location in the program data storage area. When the start address is read out from the program data storage area, the quantized data are successively read out from the quantized data storage area and are successively loaded in the data register. When the stop code is read out from the quantized data storage area, a read/write control circuit inhibits the loading of data into the data register. The quantized data loaded onto the data register are converted into analog voice signals by a D/A converter circuit.

14 ... semiconductor memory
A ... analog signals
B ... one-chip IC
17 ... D/A converter circuit
16 ... data register
20 ... read/write control circuit
15 ... address decoder
18 ... control register

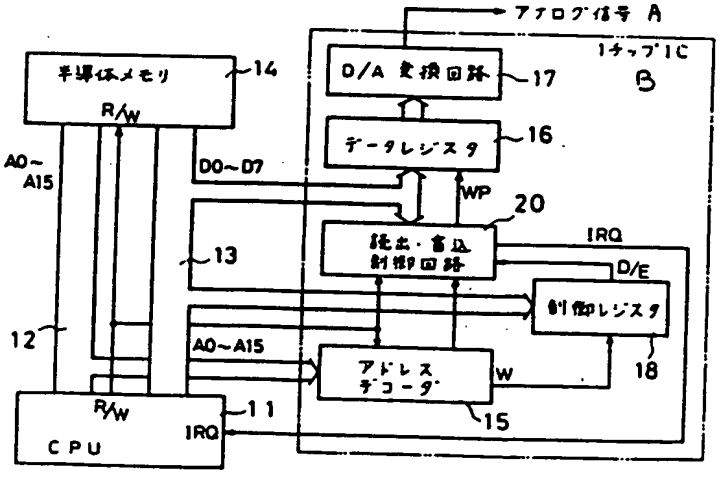

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FIG. 1

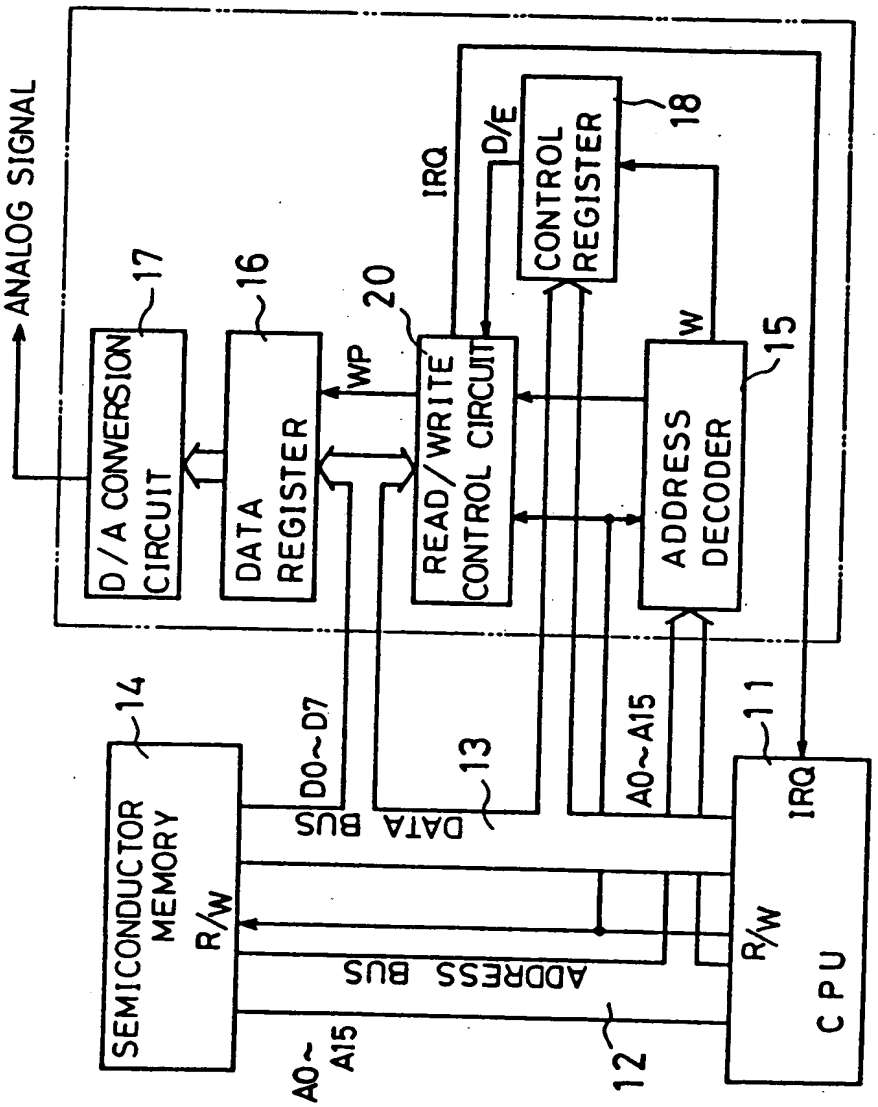

ANALOG SIGNAL
D/A CONVERSION CIRCUIT
17
DATA REGISTER
16
WP
20
READ/WRITE CONTROL CIRCUIT
IRQ
D/E
CONTROL REGISTER
18
W
ADDRESS DECODER
15
SEMICONDUCTOR MEMORY
R/W
14
D0~D7
BUS
DATA
13
A0~A15
11
IRQ
R/W
CPU
ADDRESS BUS
A0~A15
12

FIG. 2

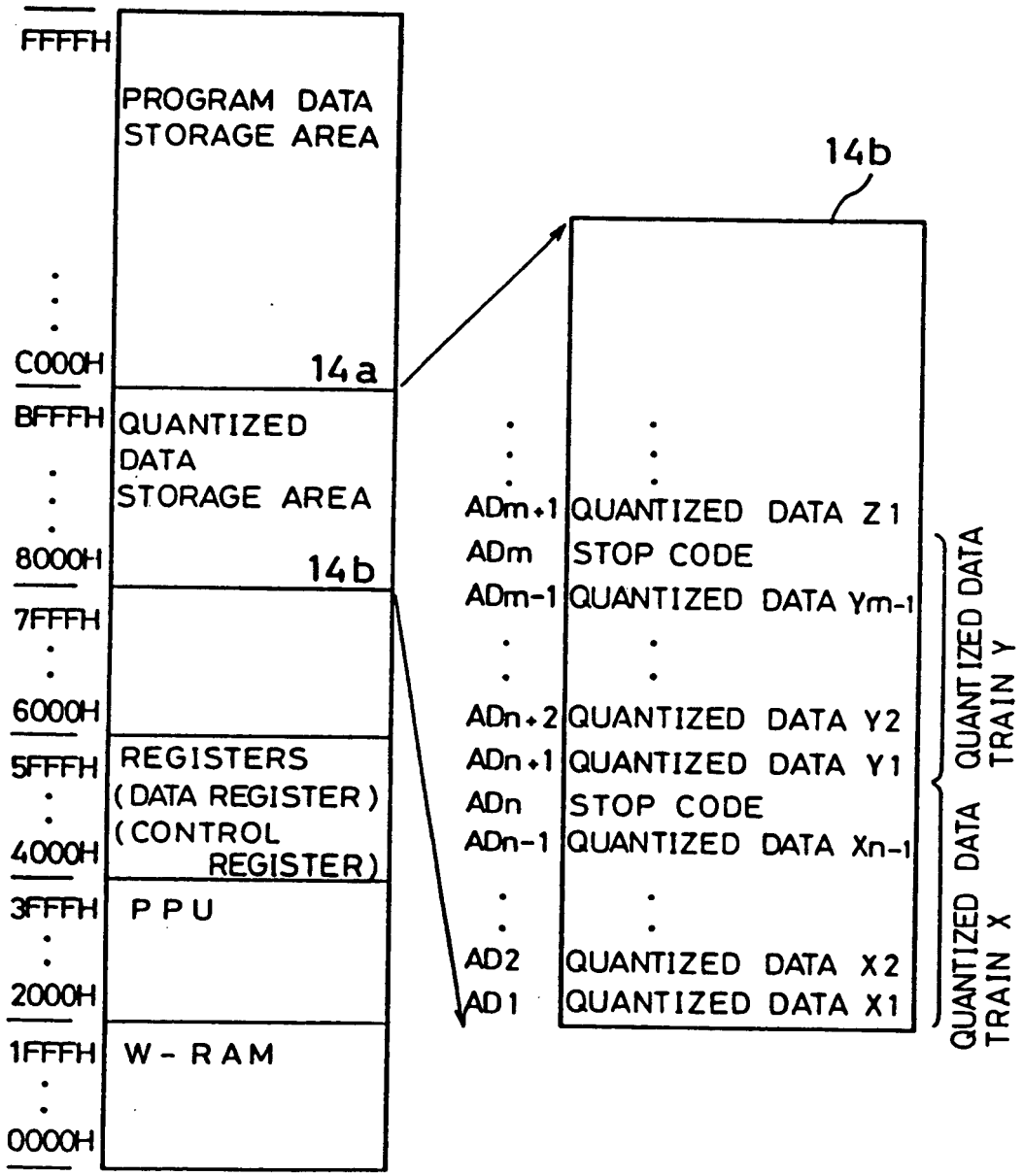

FFFFH
PROGRAM DATA STORAGE AREA
C000H
14a
BFFFH
QUANTIZED DATA STORAGE AREA
8000H
14b
7FFFH
6000H
5FFFH
REGISTERS (DATA REGISTER) (CONTROL REGISTER)
4000H
3FFFH
PPU
2000H
1FFFH
W-RAM
0000H
14b
ADm+1 QUANTIZED DATA Z1
ADm STOP CODE
ADm-1 QUANTIZED DATA Ym-1
ADn+2 QUANTIZED DATA Y2
ADn+1 QUANTIZED DATA Y1
ADn STOP CODE
ADn-1 QUANTIZED DATA Xn-1
AD2 QUANTIZED DATA X2
AD1 QUANTIZED DATA X1
QUANTIZED DATA TRAIN Y
QUANTIZED DATA TRAIN X

FIG. 3

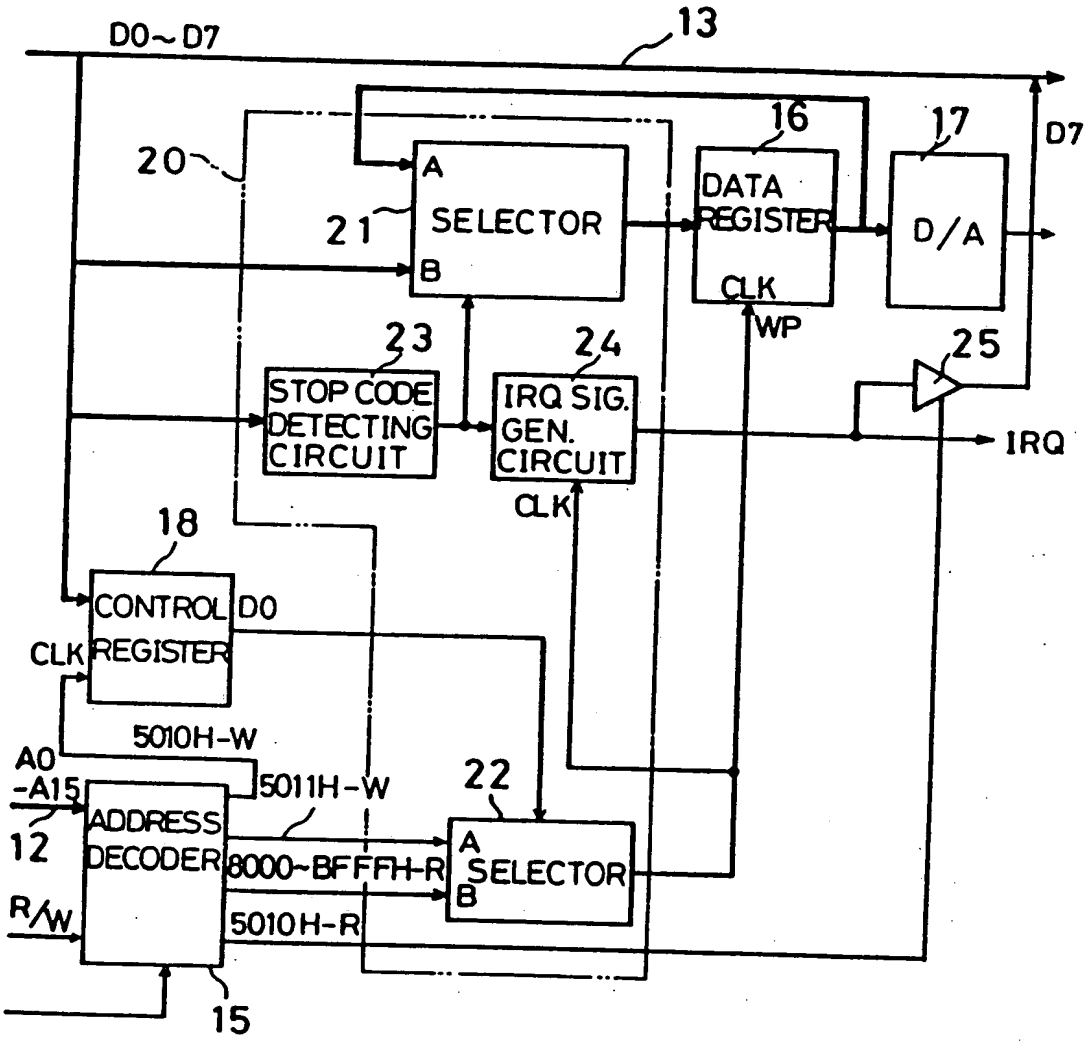

D0~D7
13
20
21
A
SELECTOR
B
16
DATA REGISTER
CLK
WP
17
D/A
D7
23
STOP CODE DETECTING CIRCUIT
24
IRQ SIG. GEN. CIRCUIT
CLK
25
IRQ
18
CONTROL REGISTER
D0
CLK
5010H-W
A0
-A15
12
ADDRESS DECODER
5011H-W
8000~BFFFH-R
5010H-R
R/W
22
A
SELECTOR
B
15

FIG. 4

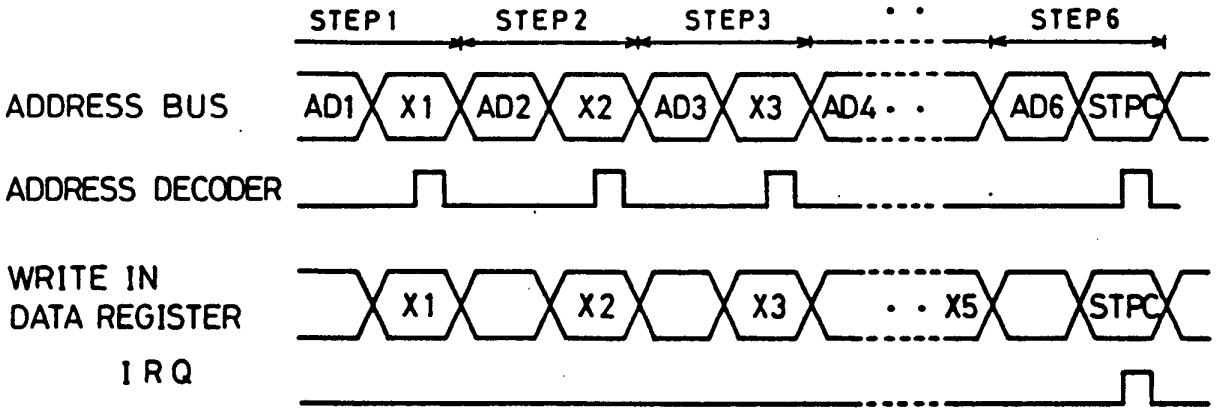

STEP1
STEP2
STEP3
STEP6
ADDRESS BUS
AD1
X1
AD2
X2
AD3
X3
AD4
AD6
STPC
ADDRESS DECODER
WRITE IN
DATA REGISTER
X1
X2
X3
X5
STPC
IRQ

FIG. 5

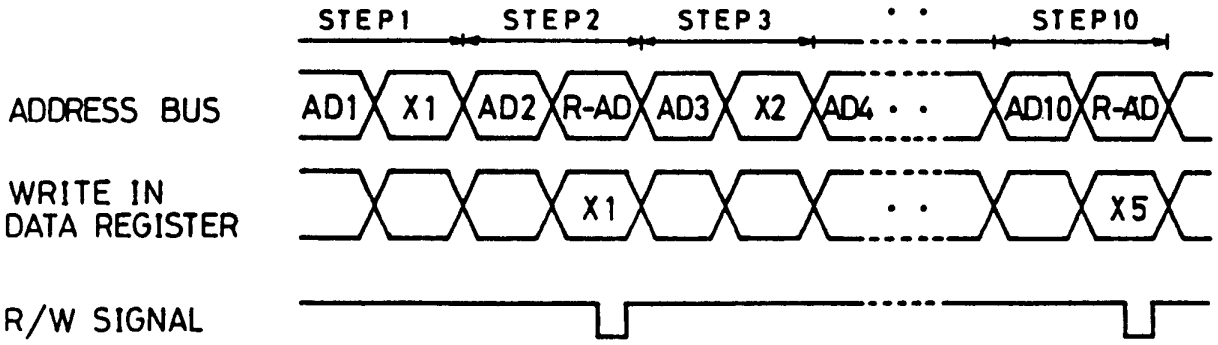

STEP1
STEP2
STEP3
STEP10
ADDRESS BUS
AD1
X1
AD2
R-AD
AD3
X2
AD4
AD10
R-AD
WRITE IN
DATA REGISTER
X1
X5
R/W SIGNAL

FIG. 6

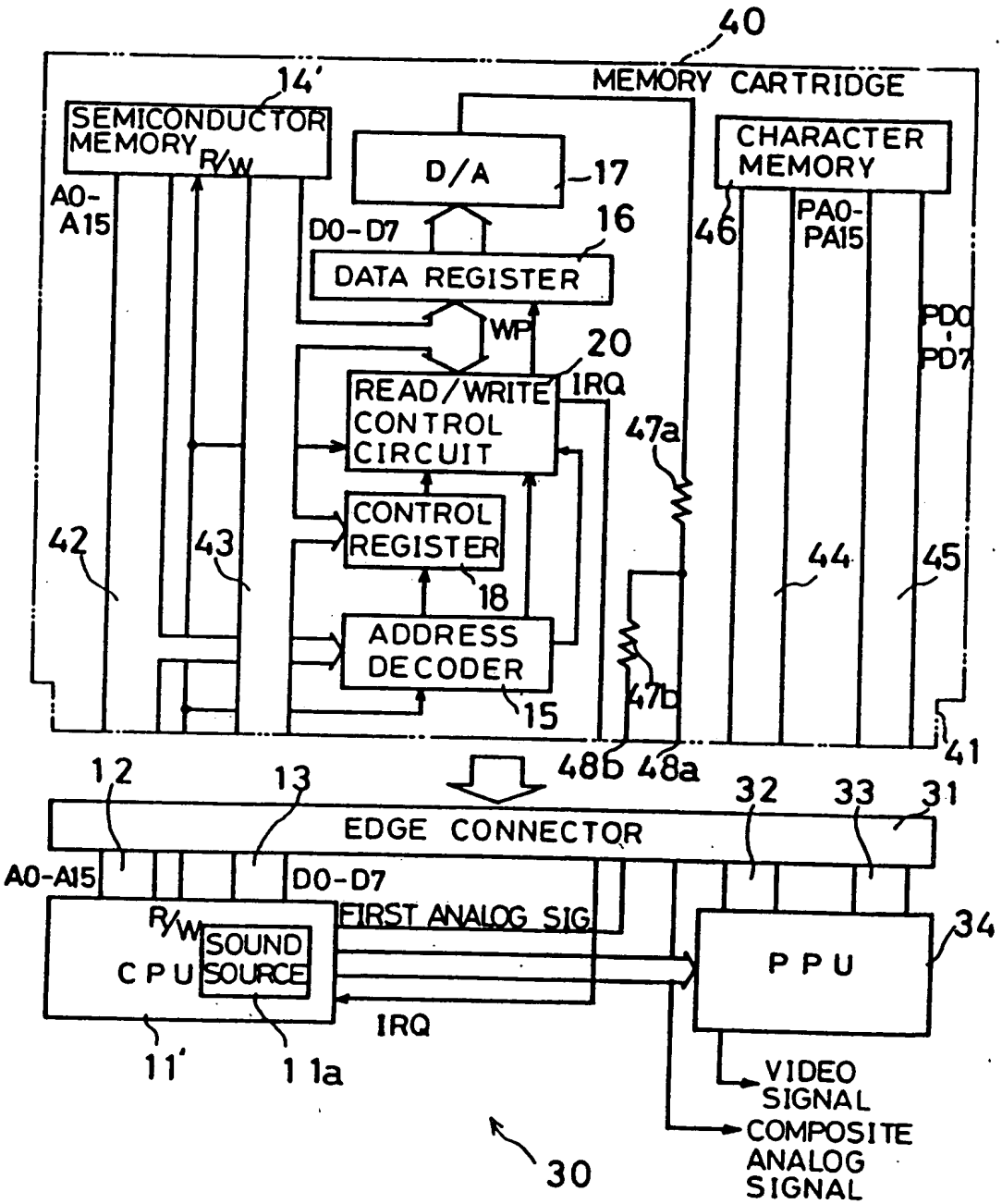
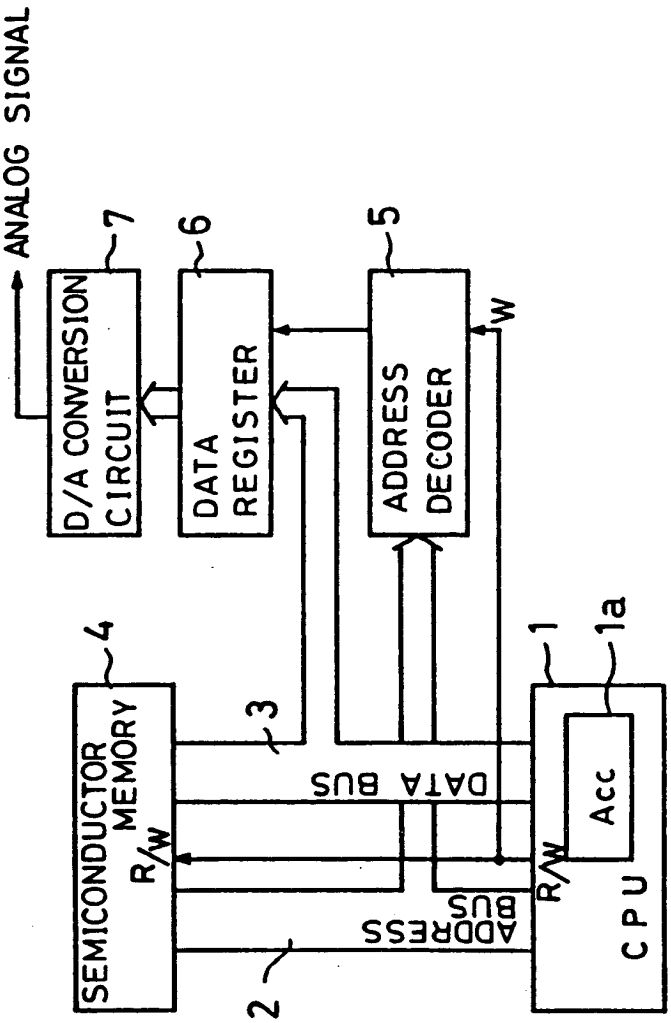

40
MEMORY CARTRIDGE
14'
SEMICONDUCTOR MEMORY
R/W
A0-A15
D/A
17
D0-D7
16
DATA REGISTER
WP
20
IRQ
READ/WRITE CONTROL CIRCUIT
CONTROL REGISTER
18
ADDRESS DECODER
15
42
43
47a
47b
CHARACTER MEMORY
46
PA0-PA15
PD0-PD7
44
45
41
48b
48a
12
13
32
33
31
EDGE CONNECTOR
A0-A15
D0-D7
R/W
SOUND CPU
SOURCE
FIRST ANALOG SIG
IRQ
PPU
34
11'
11a
VIDEO SIGNAL
COMPOSITE ANALOG SIGNAL
30

FIG. 7


ANALOG SIGNAL
D/A CONVERSION CIRCUIT
7
DATA REGISTER
6
ADDRESS DECODER
5
W
SEMICONDUCTOR MEMORY
R/W
4
3
DATA BUS
ADDRESS BUS
2
1
1a
Acc
R/W
C P U

2249839

Specification

Digital Sound Source Apparatus And External Memory Cartridge Used Therefor

Technical Field

The present invention relates to a digital sound source apparatus and an external memory cartridge used therefor. More particularly, the present invention relates to a digital sound source apparatus in which quantized data associated with sounds such as music and a sound effect are stored in a memory and an analog signal for outputting a sound is generated on the basis of the quantized data in, for example, a television game set, and an external memory cartridge used therefor.

Prior Art

A digital sound source apparatus conventionally known includes one having a circuit configuration shown in Fig. 7. In Fig. 7, a semiconductor memory (merely referred to as "memory" hereinafter) 4 storing quantized data which becomes as a sound source is connected to a central processing unit (referred to as "CPU" hereinafter) 1 through an address bus 2 and a data bus 3. When an analog signal for outputting a sound is generated by reading the quantized data stored in the

memory 4 and subjecting the same to digital-to-analog conversion, the following processing is carried out.

First, in a first step, the CPU 1 applies to the memory 4 address data of an address in which the first quantized data of a certain sound is stored and at the same time, brings a read signal R into a high level, thereby to read the first quantized data and load the same into an accumulator 1a. In a second step, the CPU 1 generates address data which designates a data register 6 to apply the same to an address decoder 5 and then, outputs a write signal W and outputs onto the data bus 3 the quantized data loaded into the accumulator 1a. Responsively, the address decoder 5 decodes the address data, thereby to detect designation of writing into the data register 6 and apply a write pulse WP to the data register 6. As a result, the data register 6 reads the quantized data, and temporarily stores the quantized data until a next write pulse and quantized data are applied. The quantized data stored in the data register 6 is applied to a digital/analog (referred to as "D/A" hereinafter) conversion circuit 7 and is converted into an analog signal by the D/A conversion circuit 7, to be outputted to, for example, an amplifier circuit (not shown) separately connected.

Such an operation is performed at every time when

quantized data stored in each of addresses in a quantized data storage area of the memory 4 is read.

According to the prior art, the CPU 1 must sequentially perform operations such as (1) addressing of the external memory 4, (2) outputting of a read signal, (3) addressing of the data register 6, and (4) outputting of a write signal so as to read quantized data from a certain address and convert the same into an analog signal, so that processing time required to generate a sound becomes long. Therefore, a burden on the CPU 1 is large. In addition, since the number of program steps for generating a sound is increased, not only it takes long to develop a program but also a necessary storage capacity is increased.

Particularly when the digital sound source apparatus is applied to an information processing unit for displaying or processing an image and generating a sound, for example, a television game set, the CPU 1 for generating music, a sound effect or the like is also used for image display or an analog sound source. Accordingly, if it takes long to perform processing for generating a sound, the other capabilities such as a capability to display an image is lowered. In order to prevent the capability to display an image from being lowered, a method is considered of using a high-speed

CPU or a CPU dedicated to a sound generating circuit. In the case, however, the digital sound source apparatus is high in cost. In addition, this method is not applicable in a case where compatibility with an information processing unit being already sold is intended to be ensured.

Summary of the Invention

Therefore, a principal object of the present invention is to provide a digital sound source apparatus capable of performing processing for generating a sound with a lesser number of steps and reducing a burden on a central processing unit.

Another object of the present invention is to provide an external memory cartridge used for such a digital sound source apparatus and detachable from a central processing unit.

A digital sound source apparatus according to the present invention comprises a central processing unit for processing information in a digital manner, an address bus as well as a data bus connected to the central processing unit, a semiconductor memory connected to the address bus and the data bus, temporary storing means as well as write control means connected to the data bus, detecting means connected to the

address bus, and digital/analog converting means.

The semiconductor memory comprises a quantized data storage area for storing quantized data in a predetermined address space and a program data storage area storing program data for reading and controlling at least quantized data in response to access from the central processing unit. In the quantized data storage area, a plurality of quantized data for generating a series of sounds are stored as a quantized data train, and a stop code is stored in the last address of the quantized data train. Start address data for designating a start address of the quantized data train is stored in a certain address in the program data storage area. The temporary storing means temporarily stores quantized data applied from the data bus sequentially at every time when a write signal is applied. The detecting means detects a fact that address data applied to the semiconductor memory from the central processing unit designates the quantized data storage area. The write control means generates a write signal at every time when an output of the detecting means is obtained and applies the same to the temporary storing means and stops generation of the write signal when it detects the stop code. The digital/analog converting means sequentially converts

into an analog signal the quantized data temporarily stored in the temporary storing means.

The external memory cartridge is constructed to be attachable to or detachable from an information processing unit comprising a central processing unit for processing information in a digital manner, a first address bus and a first data bus respectively connected to the central processing unit, and a connector connected to the first address bus and the first data bus, and comprises a semiconductor memory, a printed circuit board, temporary storing means, detecting means, write control means, and digital/analog converting.

The semiconductor memory comprises a quantized data storage area for storing quantized data in a predetermined address space and a program data storage area storing program data for reading and controlling at least quantized data in response to access from the central processing unit. In the quantized data storage area, a plurality of quantized data for generating a series of sounds are stored as a quantized data train, and a stop code is stored in the last address of the quantized data train. Start address data for designating a start address of the quantized data train is stored in a certain address in the program data storage area. The printed circuit board is constructed

to be attachable to or detachable from a connector on the side of the information processing unit. A plurality of terminal portions which are connected to the first address bus and the first data bus when the external memory cartridge is inserted into the connector, and a second address bus and a second data bus for connecting the first address bus and the first data bus to the semiconductor memory through the respective terminal portions are formed on the printed circuit board. The temporary storing means is connected to the second data bus, and temporarily and sequentially stores quantized data applied from the second data bus sequentially at every time when a write signal is applied. The detecting means is connected to the second address bus and detects a fact that address data applied to the semiconductor memory from the central processing unit designates the quantized data storage area. The write control means is connected to the second data bus, and applies the write signal to the temporary storing means at every time when an output of the detecting means is obtained and stops generation of the write signal when it detects the stop code. The digital/analog converting means sequentially converts into an analog signal the quantized data temporarily stored in the temporary storing means to

output the analog signal through the terminal portions on the printed circuit board.

According to the digital sound source apparatus in the present invention, a sound can be generated in a digital manner with a lesser number of steps, thereby to make it possible to reduce the burden on the central processing unit.

According to the external memory cartridge in the present invention, construction of the information processing unit need not be altered, thereby to make it possible to maintain compatibility with a type of information processing unit being already put on the market.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

Brief Description of the Drawings

Fig. 1 is a block diagram showing a digital sound source apparatus according to one embodiment of the present invention;

Fig. 2 is an illustrative view showing a memory space of a CPU;

Fig. 3 is a detailed block diagram showing a read/write control circuit and its related circuits;

Fig. 4 is a timing chart showing an operation of the embodiment;

Fig. 5 is a timing chart showing an operation of a prior art;

Fig. 6 is a block diagram showing another embodiment of the present invention, particularly showing a main unit of a television game set to which the present invention is applied and an external memory cartridge which characterizes the embodiment; and

Fig. 7 is a circuit diagram showing one example of a conventional digital sound source apparatus.

Best Mode for Practicing the Invention

Fig. 1 is a block diagram showing one embodiment of a digital sound source apparatus according to the present invention. In particular, Fig. 1 shows a principle of a sound source apparatus.

In Fig. 1, a semiconductor memory 14 is connected to a CPU 11 through an address bus 12 and a data bus 13. The memory 14 comprises a program data storage area 14a and a quantized data storage area 14b, as represented by, for example, a memory space of 8000H (H in the last digit indicates hexadecimal notation) to FFFFH on a

memory map as viewed from the CPU shown in Fig. 2. In the quantized data storage area 14b, a plurality of quantized data (X1 - Xn-1, Y1 - Ym-1, ...) for generating a series of sounds are stored as a plurality of quantized data trains (X, Y, ...), and a stop code is stored in a last address of each of the quantized data trains (X, Y, ...). The quantized data is not limited to one obtained by quantizing music played by a musical instrument or a human voice and subjecting the same to pulse code modulation (PCM). For example, the quantized data may be one prepared with a programming method by an input device such as a keyboard.

The plurality of quantized data trains become data for generating a plurality of series of sounds by thus storing the quantized data. If a first address (that is, a start address) of a desired quantized data train is designated, quantized data are continuously and sequentially read until the stop code is detected. To this end, start address data for designating a start address of a certain quantized data train (X, Y, or the like) is stored in advance in a certain address corresponding to a timing when a sound corresponding to the a desired quantized data train is to be generated in the program data storage area 14a. In addition, a code which represents a silent sound and in which all bits

are "0" is used, for example, as the stop code.

On the other hand, an address decoder 15 is connected to the address bus 12. A data register 16, a control register 18 and a read/write control circuit 20 are connected to the data bus 13. The address decoder 15 is constructed by comprising a decoder capable of detecting an address for designating the quantized data storage area 14b. In addition, the address decoder 15 applies its detection signal to the read/write control circuit 20 at every time when address data for designating a range of the quantized data storage area 14b is changed, and applies a write pulse WP to the control register 18 when a write signal W is applied. The data register 16 is constituted by, for example, D-type flip-flops (abbreviated as "D-FF" hereinafter) of 8 bits. The control register 18 is constituted by a D-FF of one bit corresponding to a D0 bit.

The read/write control circuit 20 applies the write pulse WP to the data register 16 at every time when the detection signal representing the range of the quantized data storage area 14b is applied from the address decoder 15, loads into the register 16 quantized data applied through the data bus 13 at that time, and stops the generation of the write pulse WP when it detects the stop code to inhibit writing into the data register 16.

The details of the read/write control circuit 20 will be described later with reference to Fig. 3.

A digital/analog (abbreviated as "D/A" hereinafter) conversion circuit 17 is connected to the data register 16. The D/A conversion circuit 17 subjects the contents stored in the data register 16 (quantized data) to D/A conversion and outputting an analog signal. If an analog signal corresponding to a quantized data train is outputted, one sound is outputted.

The analog signal is applied to a speaker (not shown) through an amplifier (not shown) separately connected to be outputted as a sound.

The control register 18 is used for temporarily storing data (one bit of D0) for switching a first mode (enable; E) in which the quantized data is automatically written into the data register 16 as in the present embodiment and a second mode (disable; D) in which the CPU 11 designates a write address each time to write quantized data as done in the prior art. However, the control register 18 is not required for applications requiring no such switching of modes.

Meanwhile, it is needless to say that the address decoder 15, the data register 16, the D/A conversion circuit 17, the control register 18 and the read/write control circuit 20 may be constituted by a one-chip

integrated circuit (IC) so as to improve production efficiency and facilitate assembly.

Fig. 3 is a detailed diagram showing the read/write control circuit and related circuits. The read/write control circuit 20 comprises selectors 21 and 22, a stop code detecting circuit 23, and an interrupt (IRQ) signal generating circuit 24. When a code which represents a silent sound and in which all bits are "0" is used as the stop code, the stop code detecting circuit 23 is constituted by a decoder capable of detecting the code. The interrupt signal generating circuit 24 is constituted by, for example, a D-FF.

Description is now made of an operation of the present embodiment with reference to Figs. 1 to 3. The CPU 11 generally performs operations other than sound generation on the basis of a program set and stored in advance in the program data storage area 14a of the memory 14. However, the following operation is performed when a digital sound is generated.

Description is now made of an operation in a mode (a first mode) in which the quantized data is written into the data register 16 with one step. At a timing when a sound is to be generated, the CPU 11 applies mode designation data (for example, D0 bit data in an address of 5010H) to the control register 18 through the data

bus 13 so as to designate an operation mode of the read/write control circuit 20 as the first mode, and outputs control register designation address data (for example, 5010H) to the address bus 12, thereby to load the mode designation data into the control register 18.

Thereafter, in order to generate a sound corresponding to a certain quantized data train (for example, X), the CPU 11 presets in an address counter (not shown) address data (AD1) for designating a start address of the quantized data train X which is to be outputted so as to output the same to the address bus 12 and at the same time, outputs a read signal R. At this time, the address decoder 15 decodes the address data, detects the designation of the quantized data storage area 14b (for example, any one of addresses in a range of 8000H to BFFFH), and generates one pulse in synchronization with a system clock SCK. This pulse is applied to a B input terminal of the selector 22. Responsively, the selector 22 applies to the data register 16 a signal to an A input terminal as a write pulse WP because it receives at that time a signal (at a high level) representing the first mode from the control register 18.

On the other hand, the memory 14 outputs the quantized data X1 in response to the designation of the

start address of the quantized data train X, and applies the same to a B input terminal of the selector 21 through the data bus 13. At this time, a stop code detection output (at a high level) is not applied to the selector 21 from the stop code detection circuit 23. Accordingly, the selector 21 selects the quantized data X1 from the B input terminal and applies the same to the data register 16. Consequently, the data register 16 loads (temporarily stores) the quantized data X1. This quantized data X1 is subjected to D/A conversion by the D/A converter 17 and is outputted as an analog signal.

Subsequently, the CPU 11 increments an address counter (not shown) to generate address data for designating next quantized data X2, and outputs the same to the address bus 12. Responsively, the address decoder 15 detects the designation of the quantized data storage area 14b and outputs one pulse in synchronization with a system clock SCK. This pulse is applied as the write pulse WP to the data register 16 through the selector 22. At the same time, the quantized data X2 is read from the memory 14 and is applied to the B input terminal of the selector 21 through the data bus 13, to be an input of the data register 16. Therefore, the data register 16 loads the quantized data X2.

In the same manner hereafter, the write pulse WP is applied to the data register 16 at every time when the address data for designating the quantized data storage area 14b is changed by sequentially designating addresses of the quantized data train X, and the quantized data as addressed is read, so that the quantized data are sequentially stored in the data register 16. Thus, the quantized data Xl to Xn sequentially stored in the data register 16 are subjected to D/A conversion by the D/A converter 17 and are outputted as analog signals. A series of quantized data (that is, data in the quantized data train X) are outputted as an analog signal, thereby to generate one sound or music.

When the CPU 11 designates the last address (ADn+1) of the quantized data train X, the stop code is read from the memory 14. This stop code is applied to the selector 21 and the stop code detecting circuit 23 through the data bus 13. At this time, in the same manner as the above described operation, the address decoder 15 generates one pulse and the selector 22 outputs the write pulse WP. Accordingly, the data register 16 loads the stop code. The stop code detecting circuit 23 detects the stop code in response to reading of the stop code and applies an output at a

high level to the selector 21. Therefore, the selector 21 hereafter applies data from an A input terminal to the data register 16. Consequently, the stop code (data in which all bits are "0") continues to be loaded into the data register 16 while circulating through the data register 16 and the selector 21. As a result, the D/A conversion circuit 17 continuously outputs analog signals at a zero level, resulting in a silent state.

At the same time, the interrupt signal generating circuit 24 generates an interrupt (IRQ) signal in response to application of the output at a high level from the stop code detecting circuit 23 and the clock pulse from the selector 22, and continues to generate the IRQ signal until the stop code detecting circuit 23 detects data other than the stop code and brings its output into a low level.

On the other hand, the CPU 11 generates an address (for example, 5010H-R) for designating reading of an interrupt signal at a timing when the presence or absence of the interrupt signal is to be detected on the basis of program processing. Responsively, the address decoder 15 generates a signal designating reading of an interrupt signal to open a gate circuit 25. Accordingly, the gate circuit 25 outputs the IRQ signal to the data bus 13. As obvious from the embodiment

shown in Fig. 1, when the IRQ signal is directly applied to the CPU 11 without passing through the data bus 13, the gate circuit 25 is not required.

Furthermore, when a sound is generated on the basis of the quantized data Y1 to Ym in the quantized data train Y, the CPU 11 designates a start address (An+1) and then, sequentially increments the address to (An+2) to Am, thereby to perform the same operation. However, setting of the mode in which the CPU 11 writes each quantized data into the data register 16 with one step is not required provided that the mode once set must be changed.

Meanwhile, the embodiment shown in Fig. 3 is so constructed as to allow switching between the first mode in which the CPU 11 writes each quantized data into the data register 16 with one step and the mode (second mode) in which the CPU 11 writes each quantized data into the data register 16 with two steps in the same manner as the prior art shown in Fig. 7 so as to also allow a sound to be generated in the conventional system shown in Fig. 7. Description is now made of an operation in the second mode in which quantized data is written with two steps.

In the second mode, data for designating the second mode (for example, logical "0") is set in a D0 bit of an

address (for example, 5010H) corresponding to the control register 18. The CPU 11 designates the address 5010H prior to reading of quantized data and loads in advance second mode designation data into the control register 18. In this case, the control register 18 does not output an enable signal (that is, outputs a disable signal at a low level), so that the selector 22 is disabled. Consequently, even if data which represents a silent sound and in which all bits are "0" (corresponding to the stop code) is read from the memory 14, the interrupt signal generating circuit 24 does not generate an IRQ signal.

When the second mode is used in which each quantized data is written into the data register 16 with two steps, read address data, and write address data for designating writing into the data register 16 of quantized data are programmed in the program data storage area 14a with two steps, and no stop code is programmed at the end of each quantized data train in the quantized data storage area 14b. The CPU 11 designates an address storing the read address data of certain quantized data in the first step, thereby to read the quantized data from the address and load the same into an accumulator (not shown).

Thereafter, the CPU 11 outputs address data (5011H-

W) for designating writing into the data register 16 in the second step. This address data is detected by the address decoder 15, and the address decoder 15 applies a decode output to the A input terminal of the selector 22. The selector 22 generates a write pulse WP at every time when an input signal is applied to the A input terminal and applies the same to the data register 16. Therefore, quantized data is read from the memory 14 to be applied to the selector 21 through the data bus 13. The selector 21 selects the quantized data applied to the B input terminal and applies the same to the data register 16. Accordingly, the data register 16 loads this quantized data.

The above described operation of writing quantized data to the data register 16 with two steps is performed for each quantized data. An operation of the D/A conversion circuit 17 is the same as that in the first mode in which quantized data is written with one step and hence, description thereof is omitted.

Meanwhile, on the program design, when the present invention is used for applications in which the same second mode as that in the prior art is not required, no mode switching circuit using the control register 18 and setting of program data for switching modes are required.

Referring now to the following tables 1 and 2 and Figs. 4 and 5, description is made of a reason why the burden on the CPU 11 in the first mode can be reduced, as compared with that in the second mode.

Table 1

address	instruction	operand	cycle
AD 1	LDA	X 1	4
AD 2	LDA	X 2	4
AD 3	LDA	X 3	4
AD 4	LDA	X 4	4
AD 5	LDA	X 5	4
AD 6	LDA	STPC	4
AD 7	-	-	-
AD 8	-	-	-
AD 9	-	-	-
AD10	-	-	-

Table 2

address	instruction	operand	cycle
AD 1	LTA	X1	4
AD 2	STA	R-AD	4
AD 3	LDA	X2	4
AD 4	STA	R-AD	4
AD 5	LAD	X3	4
AD 6	STA	R-AD	4
AD 7	LDA	X4	4
AD 8	STA	R-AD	4
AD 9	LDA	X5	4
AD10	STA	R-AD	4

The table 1 and Fig. 4 show the operation in the first mode, and the table 2 and Fig. 5 show the operation in the second mode.

Consider a case where one sound is expressed by five quantized data, as shown in the table 1. In the first mode, quantized data X1 to X5 are sequentially stored as operands in addresses AD1 to AD5, and a stop code (STPC) is stored in an address AD6 just behind the addresses AD1 to AD5. In the second mode, quantized data X1 to X5 and data R-AD for designating writing into the data register are alternately stored as operands sequentially in addresses AD1 to AD10. In this case, an

instruction word "LDA" indicates a read instruction of data, and an instruction word "STA" indicates a load instruction into the data register. In the example as shown, description is made of a case where one step is carried out in four cycles of a machine clock.

Comparison is made between Figs. 4 and 5. In the first mode, the read address is designated in the first half of a one step period (four cycles), and the quantized data is read and at the same time, is written into the data register 16 in the second half thereof. On the other hand, in the second mode, the read address is designated in the first half of an odd step period and the quantized data loaded into the accumulator is written in the second half thereof, and a write address is designated in the first half of an even step period and the quantized data loaded into the accumulator is read and at the same time, is written into the data register 16 in the second half thereof.

Consequently, in the first mode according to the present embodiment, the number of program steps may be approximately one-half that in the conventional system, that is, in the second mode. Accordingly, processing time required to generate a sound can be reduced to approximately half, thereby to make it possible to significantly reduce the burden on the CPU 11. In

addition, if the burden on the CPU 11 is selected to the same extent, the CPU 11 can be utilized for other processing by reducing processing time required to generate a sound. In addition, the first mode has the advantage that since the number of program steps can be reduced, time and labor required to develop a program can be reduced. Such an effect or advantage is very efficient in an information processing unit so adapted as to simultaneously carry out control for image display and processing for generating a sound in, for example, a television game set. Description is now made of a case where the present invention is applied to a television game set.

Fig. 6 is a block diagram showing another embodiment of the present invention, particularly showing a main unit of a television game set 30 to which the present invention is applied and an external memory cartridge 40 which characterizes the embodiment.

In Fig. 6, the main unit of the television game set 30 comprises a CPU 11', and the CPU 11' comprises an analog sound source circuit 11a. The analog sound source circuit 11a comprises four types of sound generators for generating two types of square waves, a triangular wave and a sine wave. An output of the analog sound source circuit 11a is provided as a first

analog signal, and is introduced into the external memory cartridge 40 as described later through an edge connector 31.

On the other hand, an edge connector 31 is connected to the CPU 11' through a first address bus 12 and a first data bus 13. A picture processing unit (abbreviated as "PPU" hereinafter) 34 is connected to the edge connector 31 through an address bus 32 for image processing and a data bus 33 for image processing. The PPU 34 generates dot data which is synchronized with the scanning of a scan type display on the basis of character data applied from a character memory 46 as described later and outputs the same as an image signal under the control of the CPU 11', which uses the technique disclosed in, for example, Japanese Patent Laid-Open Gazette No. 11814/1984 (corresponding U. S. Patent No. 4,824,106).

The external memory cartridge 40 is constructed detachably from the edge connector 31, and comprises a printed circuit board 41 having a plurality of terminals electrically connected to the main unit when it is loaded on the edge connector 31. A second address bus 42 connected to the first address bus 12, a second data bus 43 connected to the first data bus 13, an address bus 44 connected to the PPU address bus 32, and a data

bus 45 connected to the PPU data bus 33 are respectively formed on the printed circuit board 41. A memory 14', an address decoder 15, a data register 16, a control register 18, and/or a read/write control circuit 20 are respectively connected to the second address bus 42 and/or the second data bus 43, as in the embodiment shown in Fig. 1. The character memory 46 is connected to the address bus 44 and the data bus 45.

The memory 14' comprises a program data storage area 14a' and a quantized data storage area 14b. Quantized data used for a digital sound source is stored in the quantized data storage area 14b as in the embodiment shown in Fig. 1. Data for generating a sound in an analog manner by the analog sound source circuit 11a is stored in addition to program data for controlling the PPU 34 to display an image in the program data storage area 14a'. For example, the program data storage area 14a' stores sound type data for designating the selection of any one of the four types of sound generators or a combination of the sound generators, and data on a frequency, a waveform or the like for designating a musical interval or a tone. If the data for an analog sound source are not only stored individually but also so programmed that they can be outputted in synchronization with quantized data, two

series of sounds for an analog sound source and a digital sound source can be generated in combination, so that a varied sound can be generated, which is effective as a sound effect. In addition, program data for returning to the original operation for image display when an IRQ signal is applied can be also set and stored in the program data storage area 14a'.

In order to output a second analog signal which is an output of the A/D conversion circuit 17 in combination with a first analog signal which is an output of the sound source circuit 11a, a conductive pattern from an output end of the A/D conversion circuit 17 is formed so as to extend to a terminal 48a on an edge portion of the printed circuit board 41 through a resistor 47a. In addition, a conductive pattern formed through a terminal 48b at a position corresponding to an output line of the first analog signal from the analog sound source circuit 11a and a resistor 47b is connected to the terminal 48a. Consequently, the first analog signal and the second analog signal are combined with each other on the printed circuit board 41 and then, is derived from the television game set 30 through the edge connector 31. Meanwhile, operations of the address decoder 15, the data register 16, the A/D conversion circuit 17, the control register 18, and the read/write

control circuit 20 in the present embodiment are the same as those in the embodiment shown in Fig. 1 and hence, description thereof is omitted.

The construction of the embodiment shown in Fig. 6 has the advantage that a digital sound source can be added on the side of the external memory cartridge 40 without altering a circuit configuration of the existing television game set 30, thereby to make it possible to achieve a sound source which varies in tone and type of sounds while maintaining compatibility with the existing television game set 30. Therefore, it is possible to also generate a language, complicated music, and a sound like synthesizer by the combination with a digital sound which cannot be generated by the conventional television game set.

Although the present invention has been described and illustrated in detail, it si clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

WHAT IS CLAIMED

1. A digital sound source apparatus comprising:

a central processing unit for processing information in a digital manner;

an address bus connected to said central processing unit;

a data bus connected to said central processing unit;

a semiconductor memory connected to said address bus and said data bus and having a quantized data storage area for storing quantized data in a predetermined address space and a program data storage area for storing program data for reading and controlling at least the quantized data in response to access from said central processing unit, said semiconductor memory storing a plurality of quantized data for generating a series of sounds as a quantized data and a stop code in a last address of the quantized data train in said quantized data storage area, and start address data for designating a start address of the quantized data train in a certain address in said program data storage area;

temporary storing means connected to said data bus for temporarily and sequentially storing the quantized data applied from said data bus at every time when a

write signal is applied;

detecting means connected to said address bus for detecting a fact that address data applied to said semiconductor memory from said central processing unit designates said quantized data storage area;

write control means connected to said data bus for generating the write signal in response to an output of said detecting means to apply the same to said temporary storing means and stopping generation of the write signal in response to detection of said stop code; and

digital/analog converting means for sequentially converting into an analog signal the quantized data temporarily stored in said temporary storing means.

2. A digital sound source apparatus according to claim 1, wherein said write control means includes stop code detecting means for detecting said stop code and further includes inhibiting means for applying an interrupt signal to said central processing unit in response to an output of said stop code detecting means to inhibit addressing of said quantized data storage area.

3. A digital sound source apparatus according to claim 2, wherein said semiconductor memory further stores image processing data for causing said central processing unit to execute arithmetic operation

processing for displaying an image, and said central processing unit is switched to execution of the arithmetic operation processing for displaying an image on the basis of the image processing data in response to application of the interrupt signal from the inhibiting means of said write control means.

4. An external memory cartridge detachably loaded to an information processing unit which comprises a central processing unit for processing information in a digital manner, a first address bus and a first data bus respectively connected to said central processing unit, and a connector connected to said first address bus and said first data bus, comprising:

a semiconductor memory having a quantized data storage area for storing quantized data in a predetermined address space and a program data storage area storing program data for reading and controlling at least the quantized data in response to access from said central processing unit, said semiconductor memory storing a plurality of quantized data for generating a series of sounds as a quantized data train and a stop code in a last address of the quantized data train in said quantized data storage area, and start address data for designating a start address of the quantized data train in a certain address in said program data storage

area;

a printed circuit board attachable to or detachable from said connector, said printed circuit board being formed with a plurality of terminal portions which are connected to said first address bus and said first data bus when the external memory cartridge is inserted into the connector, and a second address bus and a second data bus for connecting said first address bus and said first data bus to said semiconductor memory through respective terminal portions;

temporary storing means mounted on said printed circuit board and connected to said second data bus for temporarily and sequentially storing the quantized data applied from said second data bus sequentially at every time when a write signal is applied;

detecting means connected to said second address bus for detecting a fact that address data applied to said semiconductor memory from said central processing unit designates said quantized data storage area;

write control means connected to said second data bus for applying the write signal to said temporary storing means in response to an output of said detecting means and stopping generation of the write signal in response to detection of said stop code; and

digital/analog converting means for sequentially

converting into an analog signal the quantized data temporarily stored in said temporary storing means and outputting the analog signal through said terminal portions on said printed circuit board.

Published 1982 at The Patent Office, Concept House, Cardiff Road, Newport, Gwent NP9 1RH. Further copies may be obtained from Sales Branch, Unit 6, Nine Mile Point, Cwmfelinfach, Cross Keys, Newport, NP1 7HZ. Printed by Multiplex techniques ltd. St Mary Cray, Kent.

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